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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,597	10/01/2003	Peter Beer	W&B-INF-1951	7989

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EXAMINER	
MAI, SON LUU	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,597	BEER, PETER	
	Examiner	Art Unit	
	Son L. Mai	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment filed 02-15-06 has been entered. Accordingly claims 1-8 are pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakada (U.S. Patent 5,148,396).

Regarding claims 1 and 7, Nakada discloses a memory circuit, comprising: a memory cell array (figure 3) including a plurality of memory cells, said memory cell array including a plurality of word lines and a plurality of bit lines for addressing said plurality of memory cells, said memory cells disposed at crossover points of said words lines with said bit lines (memory cells, bit lines, and word lines are inherent in a memory array); a plurality of write amplifiers (101-104) for writing to said plurality of memory cells, each one of said plurality of write amplifiers assigned lines to a group of said plurality of bit lines (bit lines in a memory cell array S1 are assigned to a write amplifier 104); and an address decoding circuit (80) for simultaneously activating group of said plurality of write amplifiers (see column 4, line 56 through column 5, line 11), depending on a test mode signal (Φ3 is "1"), so that said group of said plurality of write amplifiers writes a test datum to a group of said plurality of memory cells via respectively assigned

ones of said plurality of bit lines by masking a part of an address of the bit lines which is responsible for selection of a y-segment of the memory cell array (by write mask decoder 80; see column 5, lines 43-65).

Regarding claim 2, Nakada teaches the circuit further comprises: plurality of switching devices (121-124 in figure 8); each one of said plurality of write amplifiers (111-114 in figure 8) connected to assigned ones of said plurality of bit lines via respective one of said plurality switching devices in order to write the test datum from an activated one of said plurality write amplifiers to an addressed memory cell via one of said plurality of bit lines addressed by a write address (A1A2; see column 7, line 49 through column 8, line 13).

Regarding claim 3, Nakada teaches said address decoding circuit (80 in figure 3) is configured to simultaneously connect one of said plurality of write amplifiers to assigned ones of said plurality of lines depending on the test mode signal (Φ3).

Regarding claim 4, Nakada teaches a method for writing data to a memory circuit (figure 3), which comprises: providing a memory cell array including a plurality of memory cells; providing the memory cell array with a plurality of word lines and a plurality of bit lines for addressing the plurality of memory cells, the memory cells being disposed at crossover points of the word lines and the bit lines (memory cells, bit lines, and word lines are inherent in a memory array); providing a plurality of write amplifiers (101-104 in figure 3) for writing to the plurality of memory cells, and assigning each one of the plurality of write amplifiers to a group of the plurality of bit lines (a write amplifier 104 to S1 array); simultaneously activating a group of said plurality of write amplifiers

((see column 4, line 56 through column 5, line 11), depending on a test mode signal (Φ3 is "1"), so that the group of the plurality of write amplifiers writes a test datum to a group of the plurality of the memory cells via respectively assigned ones of the plurality of bit lines, by masking a part of an address of the bit lines which is responsible for selection of a y-segment of the memory cell array (by write mask decoder 80; see column 5, lines 43-65).

Regarding claim 5, Nakada teaches the method further comprises simultaneously connecting each amplifier in the group of the plurality of write amplifiers to assigned ones of the plurality of the bit lines for writing the test datum (see column 4, lines 56-64).

Regarding claim 6, Nakada teaches the memory circuit has a plurality of switching devices (121-124 in figure 8), each one of the plurality of write amplifiers (111-114) connected to assigned ones of said plurality of bit lines via a respective one of the plurality of switching devices for writing the test datum from an activated one of the plurality of write amplifiers to an addressed memory cell via one the plurality of bit lines addressed by a write address (A1A2), which further comprises: activating selected ones of the switching devices in dependence on the test mode signal (Φ3) via the address decoding circuit (91) sending activation signals over column selected lines connected, between the address decoding circuit (91) and the switching devices (121-124).

4. Claim 8 is rejected under 35 U.S.C. 102(b) as being anticipated by Hatakeyama (U.S. Patent 6,337,820).

Hatakeyama teaches a memory circuit in figure 2, comprising: a memory cell array (MCA) including a plurality of memory cells, said memory cell array including a plurality of word lines (WL) and a plurality of bit lines (LDB) for addressing said plurality of memory cells, said memory cells disposed at crossover points of said words lines with said bit lines; a plurality of write amplifiers (WA in figure 3) for writing to said plurality of memory cells, each one of said plurality of write amplifiers assigned to a group of said plurality of bit lines and coupled to primary sense amplifiers (S/A) by respective switching devices (DBG); and an address decoding circuit (figure 4) for simultaneously activating a group of said plurality of write amplifiers, depending on a test mode signal (Φ1); so that said group of said plurality of write amplifiers writes a test datum to a group of said plurality of memory cells via respectively assigned ones of said plurality of bit lines (see column 7, lines 1-32).

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 571-272-1786. The examiner can normally be reached on 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

04-17-06

Son L. Mai
Primary Examiner
Art Unit 2827